IN THE CLAIMS:

1	1. (currently amended) A method of forming an array of DRAM cells
1	comprising the steps of:
2	forming trench capacitors in a first set of trenches in a silicon
3	anniagn ductor substrate:
4	forming vertical transistors above said trench capacitors in said first set of
5	trenches, said vertical transistors having a transistor body region at a body
6	depth and said capacitors and vertical transistors being connected by a set
7	of buried straps formed at a strap depth in a layer of said semiconductor
8	
9	substrate; forming a second set of trenches in said semiconductor substrate, said
10	second set of trenches being disposed between members of said first set of
11	trenches, said second set of trenches having an insulating liner at said strap
12	depth, whereby potential paths between adjacent buried straps in said first
13	set of trenches are blocked from forming;
14	nitriding the interior surface of said second set of trenches, such that
15	conduction is not hindered, above said insulating liner and at said body
16	
17	depth above said strap depth and said second set of trenches contain a vertical conductive path connecting
18	body regions in said semiconductor substrate at a level above said strap
19	body regions in said semiconductor substrate at a level below
20	depth and bias regions in said semiconductor substrate at a level below
21	said strap depth.
	2 (currently amended) A method according to claim 1, further
1	2. (04120-105)
2	comprising the steps of:
3	etching said <u>second set of</u> trenches within upper and lower regions of a well, such that said upper and lower regions of said well are connected by
4	well, such that said upper and lower regions of said work and some said upper and lower regions of said work and some said upper and lower regions of said work and some said upper and lower regions of said work and some said upper and lower regions of said work and some said upper and lower regions of said work and some said upper and lower regions of said work and said upper and lower regions of said work and said upper and lower regions of said work and said upper and lower regions of said work and said upper and lower regions of said work and said upper and lower regions of said work and said upper and lower regions of said work and said upper and lower regions of said work and said upper and said u

a conductive path. 5 A method according to claim 1, further comprising the (original) 3. 1 steps of: 2 forming a liner on the interior surfaces of said second set of trenches; and 3 etching said liner on the bottom surface of said second set of trenches, so 4 that said conductive path extends to said substrate through said bottom 5 surface. 6 (original) A method according to claim 2, further comprising the 4. 1 steps of: 2 forming a liner on the interior surfaces of said second set of trenches; and 3 etching said liner on the bottom surface of said second set of trenches, so 4 that said conductive path extends to said substrate through said bottom 5 surface. 6 A method according to claim 1, further comprising the (original) 5. 1 steps of: 2 3 filling said second set of trenches with a conductive material and diffusing 4 said conductive material into said substrate. 5 A method according to claim 2, further comprising the (original) 6. 1 steps of: 2 3 filling said second set of trenches with a conductive material and diffusing

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said conductive material into said substrate.

A method according to claim 3, further comprising the (original) 7. 1 steps of: 2 3 filling said second set of trenches with a conductive material and diffusing 4 said conductive material into said substrate. 5 A method according to claim 4, further comprising the (original) 8. 1 steps of: 2 filling said second set of trenches with a conductive material and diffusing 3 4 said conductive material into said substrate. 5 A method according to claim 1, in which said substrate (canceled) 9. 1 is silicon and further comprising the steps of nitriding the interior surface 2 of said second set of trenches before said step of filling said second set of 3 trenches with a conductive material. 4 A method according to claim 2, in which said substrate (canceled) 10. 1 is silicon and further comprising the steps of nitriding the interior surface 2 of said second set of trenches before said step of filling said second set of 3 trenches with a conductive material. 4 (canceled) A method according to claim 3, in which said substrate 11. 1 is silicon and further comprising the steps of nitriding the interior surface 2 of said second set of trenches before said step of filling said second set of 3 trenches with a conductive material. 4 (canceled) A method according to claim 4, in which said substrate 12. 1 is silicon and further comprising the steps of nitriding the interior surface

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of said second set of trenches before said step of filling said second set of 3 trenches with a conductive material. 4

- A method according to claim 1, in which said second set (original) 13. of trenches are formed with a transverse dimension that is the minimum 1 2 distance permitted by lithography. 3
- An integrated circuit including an array of DRAM (withdrawn) 14. 1 cells comprising: 2
- an array of trench capacitors in a first set of trenches in a semiconductor 3 substrate; 4
- said array of DRAM cells further comprising vertical transistors above said 5
- trench capacitors in said first set of trenches, said capacitors and vertical
- 6 transistors being connected by a set of buried straps formed at a strap depth 7
- in a layer of said semiconductor substrate;
- 8 a second set of trenches in said semiconductor substrate, said second set of 9
- trenches being disposed between members of said first set of trenches, said 10
- second set of trenches having an insulating liner at said strap depth, 11
- whereby potential paths between adjacent buried straps in said first set of 12
- trenches are blocked from forming; and 13
- said second set of trenches containing a vertical conductive path 14
- connecting body regions in said semiconductor substrate at a level above 15
- said strap depth and bias regions in said semiconductor substrate at a level 16
- below said strap depth. 17
 - (withdrawn) An integrated circuit according to claim 14, in which: 15. 1
 - said second set of trenches extend between upper and lower regions of a 2
 - well and have a liner on the interior surfaces thereof, such that said upper 3
 - and lower regions of said well are connected by a conductive path that is 4

- isolated from intermediate levels of said well.
- 1 16. (withdrawn) An integrated circuit according to claim 14, in which
- said semiconductor substrate is silicon and said conductive path passes
- through a nitrided silicon surface above said liner.
- 1 17. (withdrawn) An integrated circuit according to claim 14, in which
- 2 said semiconductor substrate is silicon and said conductive path passes
- through a nitrided silicon surface above said liner.